ADIABATIC CHARGING REGISTER CIRCUIT

CIP 11/25/05 This application is a continuation of application 09/871,810 now US Patent 6,788,121.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an adiabatic charging register circuit and, in particular, relates to such a circuit which reduces power consumption associated with a clock pulse.

2. Description of the Related Art

Conventionally, an LSI circuit includes a large number of register circuits, fifty thousand or more circuits. Each register circuit comprises a D-flip flop (D-FF) or D-latch circuit. A register circuit having a D-FF or D-latch is exemplified here.

First, a register circuit having a D-FF is described.

A D-FF has a pair of D-latch circuits. Fig.17 shows an example of a D-latch circuit (page 677, "Structure and Design of a Computer", by David A. Patterson and John L. Hennessy, published by NikkeiBP). A D-latch circuit 70 in Fig.17 has a pair of NOR circuits 71 and 72 which are cross-connected to each other constituting a RS-FF (reset-set-flip-flop), and a pair of AND circuits 73 and 74. It has data input terminals D, DN in differential form, a clock input terminal CK, and data output terminals Q, QN in differential form. Each of NOR circuits 71 and 72 operates as an inverter when one of the inputs of the same is in low state, and therefore, a D-latch circuit 70 in Fig.17 operates as follows.

(1) A pair of NOR circuits 71, 72 keep a previous state when a clock input terminal CK is in low state.